328414 (28)

BE (4th Semester)

Examination, April-May 2021

Branch : AEI, EEE, EI, Et & T

DIGITAL ELECTRONIC CIRCUITS

Time Allowed : Three Hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : Attempt all questions. Part (a) of all question is compulsory. Attempt any two from part (b), (c) & (d) of all the questions.

UNIT-1

Q. 1. (a) What are unit distance code ? 2

(b) (i) Convert $(1001001.011)_2$ to its equivalent decimal number.

(ii) Find 10's complement of $(935)_{11}$.

(iii) Convert 8686 in BCD.

(iv) Convert $(250.S)_{10}$ into base 3. **7**

(c) Simplify the following Boolean function to a minimum number of literals. **7**

(i) $xy + xy'$

(ii) $(x + y)(x + y')$

(iii) $xyz + x'y + xyz$

(iv) $zx + zx'y$

(v) $(A + B)' (A' + B')'$

(vi) $y(wz' + wz) + xy$

(d) State and explain DeMorgan's Theorem of Boolean algebra. 7

UNIT-2

Q. 2. (a) Why and which code is used for labelling the cell of k-map ? 2

(b) Determine the minimized expression of the logic function given as

$f = \Sigma m\ (2, 3, 5, 7, 9, 11, 12, 13, 14, 15)$

and implement through NAND logic. 7

(c) Draw k-map for the function

$$f_\alpha = AD + BD + \bar{A}\,\bar{B}\,C$$

$$f_\beta = \bar{A}\,B + B\bar{D}$$

and hence derive the k-map for

$f_1 = f_\alpha . f_\beta$ and $f_2 = f_\alpha + f_\beta$

Simplify the maps for f_1 and f_2 and give the resulting expression in SOP form. 7

(d) Simplify the following Boolean function by using the tabulation method : 7

$$f = \Sigma (0, 1, 2, 8, 10, 11, 14, 15)$$

UNIT-3

Q. 3. (a) Explain the term Multiplexing and Demultiplexing. 2

(b) Implement a full subtractor using two half subtractor and OR gate. 7

(c) Describe operation of PLA. 7

(d) Explain the operation of four-bit Carry-Look-Ahead adder circuit. What is the merit of carry-look-ahead adder ? 7

UNIT-4

Q. 4. (a) Write difference between latch and flip-flop. 2

(b) What is race around condition for J-K flip flop ? How it can be avoided in master slave flip-flop ? 7

(c) Design a Asyncronous Decade Counter. 7

(d) Draw and describe the working of parallel-in-serial out (PISO) shift register. Explain how a number can be shifted in and out from such register. 7

UNIT-5

Q. 5. (a) What is tristate logic ? 2

(b) Give comparison among various logic families. 7

(c) Design NAND, NOR gate using CMOS logic. 7

(d) Define the following parameters : 7

(i) Noice Margin

(ii) Propagation delay

(iii) Power dissipation

(iv) Speed power product.